



PATENT
Attorney Docket No. 401191/TAKADA

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

HATAKENAKA et al.

Application No. 09/871,978

Filed: June 4, 2001

Allowed: January 4, 2006

Confirmation No.: 5265

Art Unit: 2133

Examiner: David TON

For: SEMICONDUCTOR INTEGRATED
CIRCUIT DEVICE COMPRISING RAM
WITH COMMAND DECODE SYSTEM
AND LOGIC CIRCUIT INTEGRATED
INTO A SINGLE CHIP AND TESTING
METHOD OF THE RAM WITH
COMMAND DECODE SYSTEM

SUBMISSION OF FORMAL DRAWINGS

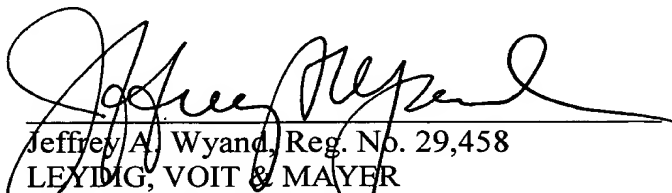
Commissioner for Patents
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Randolph Building
401 Dulany Street
Alexandria, VA 22314

Attn: Official Draftsman

Dear Sir:

Applicants enclose herewith fifteen (15) sheets of formal drawings and request that the same be made of record in this application as a substitute for the informal drawings filed with the application on June 4, 2001.

Respectfully submitted,


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